PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 : H01L 21/76

A2

(11) International Publication Number: WO 87/ 03139

(43) International Publication Date: 21 May 1987 (21.05.87)

(21) International Application Number: PCT/US86/02395

(22) International Filing Date: 10 November 1986 (10.11.86)

(31) Priority Application Number: 798,511

(32) Priority Date: 15 November 1985 (15.11.85)

(33) Priority Country: US

(71) Applicant: NCR CORPORATION [US/US]; World Headquarters, Dayton, OH 45479 (US).

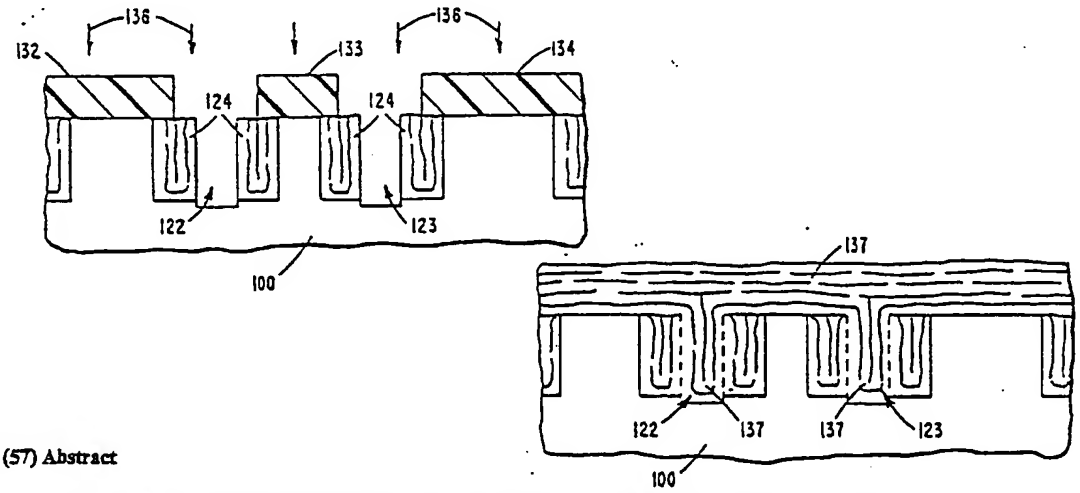
(72) Inventors: ELLSWORTH, Daniel, Lloyd ; 1424 Linden Lake Road, Fort Collins, CO 80524 (US). CRAVENS, Scott, Harris ; 4455 Hollyhock Street, Fort Collins, CO 80526 (US). MOLL, Maurice, Michael ; 742 Larkbunting Drive, Fort Collins, CO 80526 (US).

(74) Agents: SALYS, Casimer, K. et al.; Law Department, Intellectual Property Section, NCR Corporation, World Headquarters, Dayton, OH 45479 (US).

(81) Designated States: DE (European patent), FR (European patent), GB (European patent), JP, NL (European patent).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: PROCESS FOR TRENCH OXIDE ISOLATION OF INTEGRATED DEVICES



(57) Abstract

In a process for forming dielectrically filled planarized trenches (4; 138, 139) of arbitrary width in a semiconductor substrate (100), a first mask (A) defines active regions (112-114) and subdivides the trench isolation regions into a succession of the trench and plateau regions, where the widths of the trench and plateau regions fall within a dimensional range constrained by the photolithographic precision of the masks and the ability to conformally deposit dielectric material into the trenches. With the first etch mask (A) in place, the substrate (100) is anisotropically etched to form first trenches (117, 118, 119, 121). A conformal deposition of dielectric (124) follows, to form substantially void free trench dielectric, following which the surface is planarized. Next, a second mask (B), defined to be slightly larger than the active regions (112-114), is formed over the substrate (100). A selective etch is then applied to remove the plateau regions (122, 123) and thereby form new trenches approximating in depth the first trenches. A second conformal deposition of dielectric (137) follows, whereafter the surface is again planarized. The substrate surface is now planar and divided into active regions (1-3; 112-114) which are separated by oxide filled, arbitrary width trenches (4; 138, 139).

BEST AVAILABLE COPY

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FR	France	ML	Mali
AU	Australia	GA	Gabon	MR	Mauritania
BB	Barbados	GB	United Kingdom	MW	Malawi
BE	Belgium	HU	Hungary	NL	Netherlands
BG	Bulgaria	IT	Italy	NO	Norway
BJ	Benin	JP	Japan	RO	Romania
BR	Brazil	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic			SE	Sweden
CG	Congo	KR	Republic of Korea	SN	Senegal
CH	Switzerland	LI	Liechtenstein	SU	Soviet Union
CM	Cameroon	LK	Sri Lanka	TD	Chad
DE	Germany, Federal Republic of	LU	Luxembourg	TG	Togo
DK	Denmark	MC	Monaco	US	United States of America
FI	Finland	MG	Madagascar		

PROCESS FOR TRENCH OXIDE ISOLATION OF INTEGRATED DEVICES

Technical Field

This invention relates to processes of the kind for forming dielectrically filled trench regions of arbitrary width between active regions in a semiconductor substrate.

Background Art

U.S. Patent No. 4,139,442 discloses a trench isolation technique, according to which adjacent narrow trenches of fixed relationship are simultaneously formed in all trench regions. The silicon projections between adjacent trenches are thereafter converted to silicon dioxide by conventional oxidation techniques and then, if necessary, further filled with deposited oxide. However, the oxidation process has the disadvantage of being subject to the variables of volume expansion.

Disclosure of the Invention

It is an object of the present invention to provide a process of the kind specified, wherein the aforementioned disadvantage is alleviated.

Therefore, according to the present invention, there is provided a process of the kind specified, characterized by the steps of: forming on the surface of the substrate a first etch mask to cover the active regions and incrementally spaced plateau regions situated within the trench regions; etching the substrate in the presence of the first etch mask to form trenches; conformally depositing on the substrate a first dielectric layer to fill the formed trenches; planarizing the surface of the substrate; forming on the surface of the substrate a second etch mask to cover the active regions while

exposing selected incrementally spaced plateau regions; etching the selected incrementally spaced plateau regions; conformally depositing on the substrate a second dielectric layer to fill the etched plateau regions; and planarizing the surface of the substrate.

It will be appreciated that a process according to the present invention ensures the absence of conductive residue within the trench region, and provides a planar active region surface, yet is implemented without undue design or fabrication complexity. A further advantage of a process according to the invention is that the generation of the mask patterns is readily accomplished by software routines used in conjunction with computer aided design techniques. Thus the process is flexible and cost efficient. Furthermore, in a process according to the invention, mask alignment tolerances and the dimensional control requirements of the photolithographic masks are minimized.

Brief Description of the Drawings

Embodiments of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 depicts a set of active regions of differing patterns within a defined area of a substrate;

Figs. 2-7 show the interactive effects of an algorithm which subdivides the arbitrary size trench regions into trenches and plateaus of prescribed dimensions;

Fig. 8 shows the mask complement to the mask depicted in Fig. 7, which two masks are used to implement the fabrication process of the present invention; and

Figs. 9-15 are cross sectional representations of the effects on the substrate produced in the practice of the fabrication process.

Best Mode for Carrying Out the Invention

Attention is now directed to Fig. 1 of the drawings, where there is shown a portion of a substrate surface, including active regions 1, 2 and 3 separated by arbitrary width trench isolation regions 4 situated within a defined boundary 6. Preferably, the patterns represent active regions which upon the conclusion of wafer fabrication will contain integrated circuit devices, such as field effect or bipolar transistors, which are electrically isolated from one another by trench region 4.

According to the invention, the mask pattern used to create the active and trench isolation regions involves, in one aspect, the creation of two, complementary photolithographic fabrication mask patterns which have uniquely defined pattern characteristics, yet can be generated in relatively automated fashion using available design tools.

The description will first focus on the generation of the mask patterns by which the process can be exercised, and will conclude with the development of a preferred fabrication process.

Beginning with the active region patterns depicted in Fig. 1, the preferred procedure for generating the first mask, hereafter identified as Mask A, begins with the manual or automatic definition of first trench regions 7, 8, 9 and 11, to individually surround active regions 1, 2 and 3 and to project inwardly from boundary 6. Each trench region is initially defined to be approximately 1 lambda in width, as generally shown in Fig. 2. Conceptually, the operation in Fig. 2 represents the first iteration in a subdivision of the trench isolation region 4 by

moving inward from boundary 6 and outward from the boundary of each active region 1, 2 and 3, so that supplemental boundary regions, hereafter generally referred to as plateaus, are generated whenever the spacing between boundaries is 2 lambda or greater.

While lambda is determined by the minimum lithographic dimension, as will be apparent at a later point, lambda is somewhat constrained by the thickness to which a dielectric, preferably silicon dioxide, can be conformally deposited without creating voids or stress fractures when 1 to 3 lambda width trench regions are filled in and pinched off. Exemplary variables which affect the filling of such trench regions with silicon dioxide are described in U.S. Patent No. 4,104,086. With reference to such teaching, it should be understood that lambda is subject to diverse variation. The embodiment set forth hereinafter utilizes a single arbitrarily selected value for lambda to simplify the illustration of the underlying concepts.

The next iteration in the generation of the pattern for Mask A is depicted in Fig. 3 of the drawings. In this figure there is shown the addition of trench regions 12 and 13, which again are lambda or less in width. However, these trenches are separated from previously defined trench regions 7, 8, 9 and 11 by plateau regions 14 and 16, which plateau regions are also 1 lambda in width. Note, however, that the plateau region at location 17, immediately below region 13, has not been further subdivided, by virtue of the fact that the spacing between trench patterns 9 and 11 is less than 2 lambda at location 17.

The succeeding iteration in the generation of Mask A is depicted in Fig. 4 of the drawings, where those regions of formerly defined trench isolation region 4 which have not as of this time been fully subdivided are further subject to subdivision by the

formation of lambda width trenches wherever the spacing between previous trenches is 2 lambda or greater. Following this rule, the pattern depicted in Fig. 4 now includes trench region 18 of 1 lambda or less width. With the generation of the pattern depicted in Fig. 4 further subdivision will cease, in that no region remaining has a span of 2 lambda or greater.

An examination of the pattern depicted in Fig. 4 discloses that a number of trench and plateau regions defined during the preceding iterative operations are less than 1 lambda in width. For example, the plateaus at locations 19, 21 and 23 as well as the trenches at locations 12, 22 and 24. Recall that the fabrication process by which silicon dioxide is to be deposited provides a substantially planar topology only when the width of the trenches being filled is less than 3 lambda, and that only those regions greater than or equal to 1 lambda can be defined lithographically. Consequently, further refinement of the pattern depicted in Fig. 4 is necessary to compensate for the narrow trench and plateau regions. The reason the plateau regions are subject to the same lambda constraint will be apparent upon understanding the fabrication process, to be described hereinafter.

The unacceptably narrow trench and isolation regions at locations 13, 19, 21, 22 and 23 are removed by subjecting the pattern to a sequential algorithm, the end product of which is a pattern having trench and plateau regions with all widths between 1 and 3 lambda. The pattern refining technique that leads to a mask pattern having the specified constraints begins with a shrink of all trench region boundaries by an amount equal to 0.49 lambda, and the deletion of any region which shrinks to a zero dimension. The effect of this operation is to remove trench regions narrower

than 1 lambda. Directing attention to Fig. 5, the effects of this operation are depicted at locations such 26, 27 and 28, where most trench regions appear as no more than lines in the figure. The next operation is directed toward deleting plateaus which were in Fig. 4 narrower than 1 lambda. To accomplish this, the borders of the trenches are oversized by 0.98 lambda per side and the plateaus which shrink to zero are deleted. The effects of this operation appear in Fig. 6, where most plateau regions are now no more than lines, e.g. 29. The sequence of operations is concluded with another reduction in the trench pattern by 0.49 lambda per side.

The final pattern for Mask A is depicted in Fig. 7. In comparison to the pattern in Fig.4, the pattern in Fig. 7 shows that trench regions formerly narrower than 1 lambda, such as that previously located at 22, as well as plateau regions formerly narrower than 1 lambda, such as those previously at locations 19 and 23, have been removed without violating the dimensional constraint that trench and plateau regions will be between 1 and 3 lambda in width.

The complement to Mask A is Mask B, which is shown schematically in Fig. 8 of the drawings to be comprised of a pattern 1/2 lambda wider than the formerly defined active regions 1, 2 and 3, and as such is defined by respective perimeters 31, 32 and 33. The process by which the pair of masks is utilized to fabricate trench isolation regions will be fully developed in the ensuing description of the fabrication process.

An important feature of the invention, and particularly as it relates to the formation of Mask A, is the ease with which the generation of the trench and plateau patterns of the mask can be automated by using the software techniques of computer automated design.

A suitable algorithm involves a subtraction of the active region from the boundary of the established chip area, sequential undersizings by lambda followed by subtractions from the previous boundaries, a multiplicity of logical "OR" operations, and a concluding sequence of undersizing and oversizing to generate Mask A. The generation of Mask B basically involves an oversizing of the active area, but does undergo an oversizing and undersizing sequence to ensure dimensional correspondence with Mask A.

With the set of fabrication masks at hand, attention will now be directed to the process by which such masks are employed to fabricate trench oxide isolation regions of arbitrary width in substrates, where the trench isolation dielectric is preferably silicon dioxide and the substrate material is preferably monocrystalline silicon. Nevertheless, it should be understood that such materials and associated dimensional relationships are merely exemplary. Foremost, it should be appreciated that the composite invention becomes particularly valuable when it includes the combination of automated mask pattern generation with the fabrication sequence described hereinafter.

It should be understood that the mask patterns used in depicting the various steps in the fabrication process as set forth in Figs. 9-15 do not correspond to the patterns in Masks A or B, Figs. 7 and 8, but are selected to depict the central concepts of the fabrication process.

The cross section shown in Fig. 9 includes a monocrystalline silicon substrate 100, which has formed thereupon an etchant mask of photoresist formerly subjected to photolithographic processing to retain photoresist regions 101, 102, 103, 104 and 106 while exposing the substrate at locations 107, 108,

109 and 111. For purposes of this example, locations 112, 113 and 114 are defined to be the active regions, functionally corresponding to regions 1, 2 and 3 in Fig. 1. The width dimensions of photoresist regions 102 and 104 as well as the openings at 107, 108, 109 and 111 are prescribed to be approximately 1 lambda.

Upon applying the anisotropic etch 116 as depicted in Fig. 10 to substrate 100, trenches 117, 118, 119 and 121 of approximately 1 lambda width are formed into substrate 100. Monocrystalline silicon active regions 112, 113 and 114 are now separated by both trenches and supplemental plateau regions 122 and 123. Where substrate 100 is composed of monocrystalline silicon and lambda is 1 micrometer, anisotropic etch 116 is preferably performed with nitrogen trifluoride or a sulfur hexafluoride/freon mixture, and is continued until trenches 117, 118, 119 and 121 are approximately 1-4 micrometers deep. Recall that the depth and sidewide angles of the trenches are constrained by the ability to conformally deposit the silicon dioxide dielectric without voids in the succeeding steps of fabrication. Reference is again made to the teachings in U.S. Patent No. 4,104,086 for guidance. Upon the conclusion of etching, photomask segments 101, 102, 103, 104 and 106 are stripped in preparation for the deposition of the dielectric material.

The conformal deposition of dielectric follows, preferably applying the concepts described in U.S. patent No. 4,104,086 and the information set forth in the article by Levin et. al., entitled "The Step Coverage of Undoped and Phosphorus Doped SiO_2 Glass Films", which appeared in the Journal of Vacuum Science and Technology, Vol. B1(1), 1983, pages 54-61. Upon the conclusion of the conformal dielectric deposition, trenches 117, 118, 119 and 121 are filled with silicon dioxide 124 as shown in Fig. 11, the

deposition being continued until the surface topology of the deposited dielectric is substantially planar and absent of voids in the trench recesses. Where lambda is for illustration purposes set at a value of approximately 1 micrometer, and the trench is designed to have a depth of approximately 2 micrometers, the conformal deposition of dielectric preferably involves an LPCVD process using TEOS (tetraethylorthosilicon) and a deposition temperature of approximately 700 degrees C. Deposition is continued until the surface layer thickness of silicon dioxide 124 is somewhat greater than 1.5 micrometers.

To more fully appreciate the desired relationship between the width of the trenches and the thickness of the conformally deposited silicon dioxide, recall that the first mask pattern, Mask A in Fig. 7, is by design prescribed to have a width ranging between 1 and 3 lambda, herein corresponding to 1-3 micrometers. Consequently, the thickness of the conformally deposited silicon dioxide dielectric must be at least 1.5 lambda to insure trench closure, and should further include an additional margin for process variations. Preferably, the dielectric deposition would thereafter be continued for a slightly longer period to insure a more planar surface topology.

Following the deposition of silicon dioxide 124, as appears in Fig. 11, substrate 100 is subjected to an etching operation to expose surfaces 126, 127, 128, 129 and 131 of monocrystalline silicon substrate 100. Reasonable care must be exercised to ensure that the etching operation is curtailed soon after reaching the monocrystalline silicon surface. Otherwise, degradation of active region surfaces may result. The etching process may be either isotropic or anisotropic. Preferably the etchant is selective, removing silicon dioxide dielectric at a materially

greater rate than monocrystalline silicon. The specifics of such processes are well known by those who routinely practice in the art.

The substantially planar surface formed by the etching operation is then photolithographically processed to create a second etchant mask, this mask having a pattern corresponding functionally to Mask B in Fig. 8. Recall that the Mask B pattern is generally the active region oversized by approximately 1/2 lambda. As shown in Fig. 12, the formation of such a mask pattern places photoresist segments 132, 133 and 134 over respective active regions 112, 113 and 114, with slight, approximately 1/2 micron, overlaps onto previous deposits of trench oxide 124. It should be appreciated that this overlap relaxes the the alignment tolerance for the photolithographic process associated with the use of Mask B. The precision and ease of alignment for Mask B also benefits from the highly planar surface topology being processed at this stage in a fabrication cycle.

Substrate 100, with Mask B patterned photoresist segments 132, 133 and 134, is then subjected to a selective etch operation, such as etch 136 depicted in Fig. 13, to remove monocrystalline silicon in the now exposed plateau regions 122 and 123 until the depth is approximately equal to the previously etched, and now silicon dioxide 124 filled, trenches. Representative selective etching operations for a monocrystalline silicon substrate and silicon dioxide filled dielectric trenches would consist of either a dry etch involving nitrogen tri-fluoride plasma or, alternatively, a plasma having a mixture of sulfur hexafluoride and freon 12. As is suggested in Fig. 13, though the depth to which selective etch 136 removes substrate 100 is not critical, it should avoid a material undercut of oxide 124. Following the etch of monocrystalline silicon 100, masking photoresist

regions 132, 133 and 134 are stripped in conventional manner.

Fabrication of the oxide filled trenches is continued as shown in Fig. 14 by a second conformal deposition of dielectric 137 utilizing, for example, the previously described general LPCVD of silicon dioxide guidelines. Again, deposition is continued until the trenches at 122 and 123, previously plateaus of silicon, are completely filled with dielectric and the surface of the substrate approaches a substantially planar topology. The repeated application of the formerly utilized oxide deposition process is attributable to the dimensional symmetry imposed upon the trench and plateau regions during the formation of Mask A, in that those regions formerly defined as plateaus now become trenches. Consequently, the widths of trenches 122 and 123 are constrained to range between 1 and 3 lambda.

Following the formation of the substantially planar surface topology, the substrate is again subjected to either an isotropic or anisotropic etch until the active region surfaces at 126, 128 and 131 are exposed. See Fig. 15. At this point, the wafer is in a suitable form for further processing to form in such regions various active semiconductor devices isolated respectively by dielectric filled trenches 138 and 139.

On occasion it is desirable to have a high quality thermal oxide, or other dielectric material, or an impurity zone, at the trench interface between the deposited dielectric and the semiconductor substrate, for example to minimize interface state density. The present process is suitable for the practice of such alternate embodiments. For example, composite trenches 138 and 139 in Fig. 15 can be lined with a thin layer of thermally grown silicon dioxide by subjecting the substrate to a brief thermal

oxidation at a fabrication stage between anisotropic etch 116, in Fig. 10, and the conformal deposition of dielectric 124, in Fig. 11. Note that the generation of Mask A in Fig. 7, includes as a first step, in Fig. 1, the definition of trenches which establish a perimeter around each active region and, as such, ensure that any such alternate thermal oxidation operation acts in a continuum around each active region.

According to another embodiment, the walls of the trenches formed by anisotropic etch 116, Fig. 10, can be doped in conjunction with or independent of the previously noted thermal oxidation to minimize charge leakage paths along the trench surface. The use of LPCVD depositions, as depicted in Figs. 11 and 14, to fill the trench regions with dielectric avoids by virtue of the low temperatures detrimental redistributions of any such wall dopants.

In another aspect, the process is also suitable for use in the fabrication of ubiquitous wells in CMOS type devices. According to that practice, following the anisotropic etch 116 in Fig. 10 substrate 100 is subjected to doping, implemented either by a blanket implant or by a selective photoresist mask implant operation. During such implant, the relatively narrow plateau regions 122 and 123 in Fig. 10 are subjected to sidewall doping, which sidewall dopant diffuses across the plateaus of monocrystalline silicon during the well drive anneal cycle. Note that the same effect holds for narrow active regions, such as 113 in Fig. 10. In the implementation of such a procedure care must be exercised to ensure that the depth of the anneal cycle diffusion is measurably greater than 1/2 lambda. This provides a suitable interwell resistivity for ubiquitous well regions. Clearly, as the depths of trenches 117, 118, 119 and 121 increase, the

likelihood of implant scattering into the walls increases, with a concomitant decrease in the amount of impurity reaching the bottom of the well. With the plateau regions being subject to subsequent removal, it is apparent that care must be exercised to ensure that the dopant reaching the bottom of the wells is adequate upon lateral diffusion to interconnect any ubiquitous well regions having deep trench structures.

The present process as set forth in the various embodiments hereinbefore is also suitable for merger with presently practiced spin-on planarization techniques. According to such a practice, the deposition of the silicon dioxide dielectric, such as 124 in Fig. 11 or 137 in Fig. 14, would be followed by a spin-on deposition of a planarizing polymer. Thereafter, the polymer coating and upper, presumably somewhat nonplanar portion of the dielectric layer would be removed with an etchant having a 1:1 polymer-to-dielectric etch ratio.

It should be understood and appreciated that although the invention has been described in the context of using a monocrystalline silicon substrate and silicon dioxide as the trench dielectric, the fundamental aspects of the invention are not so circumscribed. It should be clear from the alternate embodiments described herein that the fundamental features of the invention are suitable for broad application to diverse semiconductor materials employing further diverse dielectrics. In all cases the invention features a trench isolation fabrication process which can be practiced without thermal oxidation, thereby avoiding adverse dopant redistributions and the associated volumetric change induced stresses, the use of but two masking levels, in which the second mask is very tolerant of misalignments and dimensional variations, the formation of the mask patterns on consistently planar surfaces, the absence

of dielectrically isolated semiconductor residuals, so as to avoid charge trapping sites and parasitic capacitance sources, a highly automated mask generation technique, and the flexibility of allowing for selective oxidation, doping or deposition to inhibit leakage currents or to define ubiquitous wells.

Claims:

1. A process for forming dielectrically filled trench regions (4; 138, 139) of arbitrary width between active regions (1-3; 112-114) in a semiconductor substrate (100), characterized by the steps of: forming on the surface of the substrate a first etch mask (A) to cover the active regions and incrementally spaced plateau regions (122, 123) situated within the trench regions (4; 138, 139); etching the substrate in the presence of the first etch mask (A) to form trenches (117, 118, 119, 121); conformally depositing on the substrate a first dielectric layer (124) to fill the formed trenches (117, 118, 119, 121); planarizing the surface of the substrate (100); forming on the surface of the substrate (100) a second etch mask (B) to cover the active regions (1-3; 112-114) while exposing selected incrementally spaced plateau regions (122, 123); etching the selected incrementally spaced plateau regions (122, 123); conformally depositing on the substrate a second dielectric layer (137) to fill the etched plateau regions (122, 123); and planarizing the surface of the substrate (100).

2. A process according to claim 1, characterized in that the incrementally spaced plateau regions (122, 123) are spaced apart from the active regions (1-3; 112-114) and the adjacent plateau regions (122, 123) by a distance of approximately 1-3 lambda, lambda being defined as a variable relating to the photolithographic precision of the etch masks (A, B) and the deposition characteristics of the dielectric (124, 137) within the trenches (117, 118, 119, 121) and etched plateau regions.

3. A process according to claim 2, characterized in that the depth to which the trenches (117,0 118, 119, 121) are formed in the substrate is related to lambda in a proportion that ensures the closure of the trenches with conformally deposited first dielectric material (124) without entrapped voids of material size.

4. A process according to claim 1, characterized in that the etching of the substrate (100) is anisotropic, and the etching of the incrementally spaced plateau regions (122, 123) is selective to remove semiconductor substrate material while minimally removing first dielectric layer material (124).

5. A process according to claim 4, characterized in that the substrate (100) is a monocrystalline silicon semiconductor; and at least one of the steps of conformally depositing on the substrate (100) first and second dielectric layers (124, 137) involves a low pressure chemical vapor deposition of silicon dioxide.

6. A process according to claim 5, characterized in that the deposition of the first layer of silicon dioxide (124) is continued until a depth of approximately 1.5 lambda plus a process variation offset is obtained.

7. A process according to claim 5, characterized in that at least one of the first and second planarizing of the surface steps includes etching with a nonselective silicon-to-silicon dioxide etchant.

8. A process according to claim 5, characterized in that at least one of the planarizing of the surface steps further includes a prior operation of applying a planarizing spin-on coating and etching of the coated surface with a nonselective spin-on coating-to-silicon dioxide etchant.

9. A process according to claim 1, characterized in that the second etch mask (B) covers the surface in regions beyond the covered active regions (112-114).

10. A process according to claim 9, characterized in that the second etch mask covers the surface approximately 0.5 lambda beyond the covered active regions (112-114).

11. A process according to claim 4, characterized in that the etching of the selected incrementally spaced plateau regions (122, 123) is continued until the depth is approximately equal to the trenches (117, 118, 119, 121) formed by the first etch.

12. A process according to claim 5, characterized in that, before the step of conformally depositing on the substrate (100) a first dielectric (124), there is effected the step of oxidizing the exposed surface of the substrate.

13. A process according to claim 2, characterized in that, before the step of conformally depositing on the substrate (100) a first dielectric layer (124), there are effected the steps of: implanting the substrate (100) with a well dopant; and diffusing the dopant to form a continuum of the well dopant in a trench region.

14. A process according to claim 13, characterized in that the substrate (100) is a monocrystalline silicon semiconductor and the step of diffusing the dopant is performed under oxidizing conditions for silicon.

15. A process according to claim 13, characterized in that the step of difussing the dopant is continued until the dopant diffuses a distance greater than 1.5 lambda.

FIG. 1

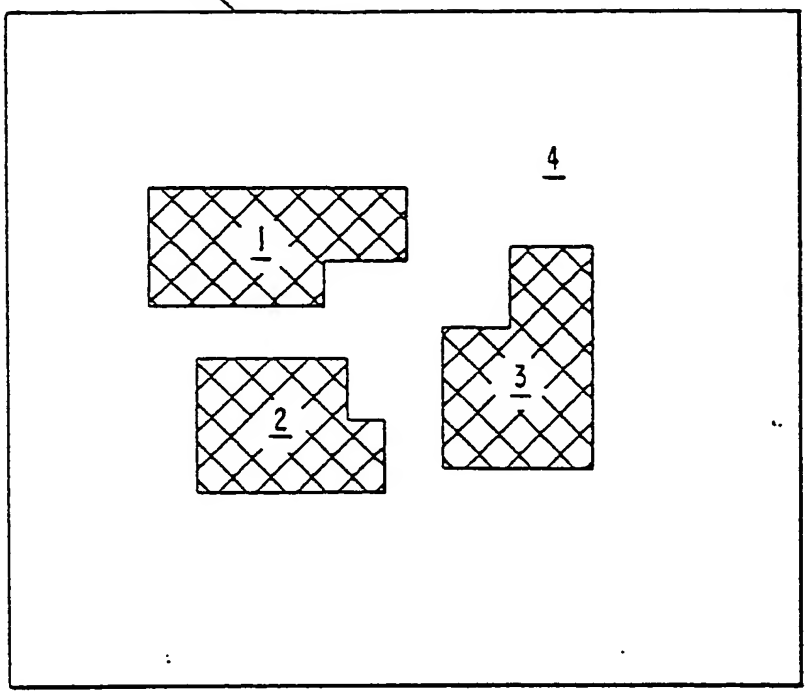


FIG. 2

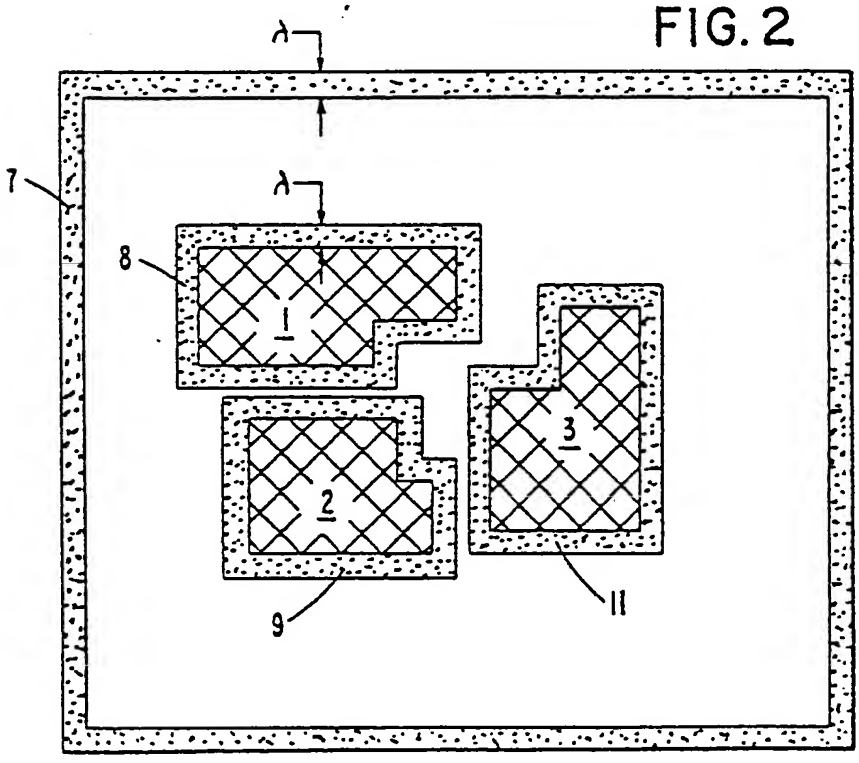


FIG. 3

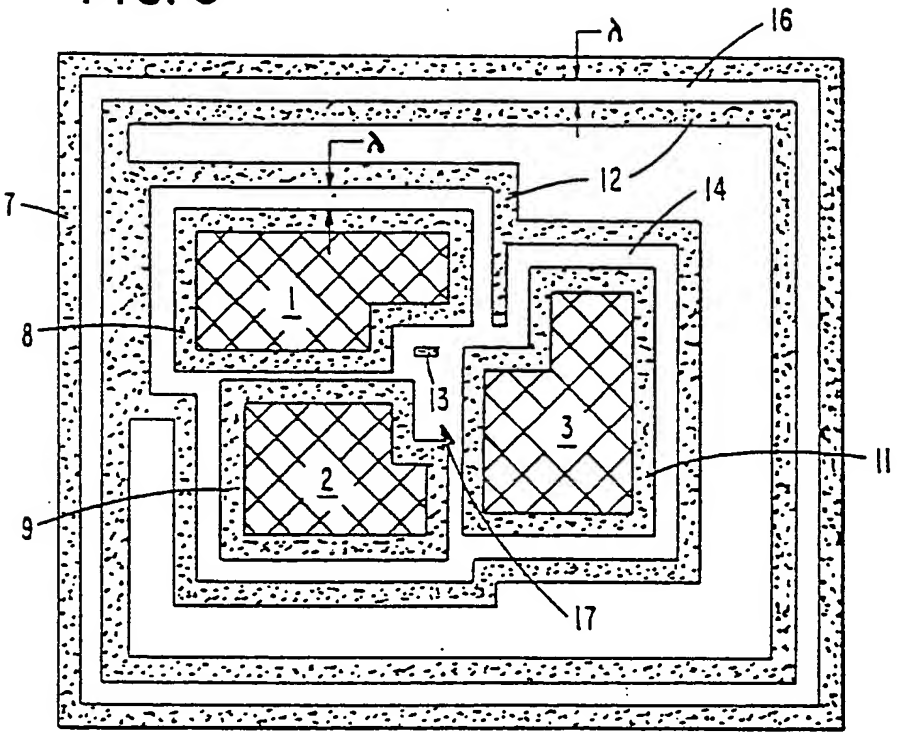


FIG. 4

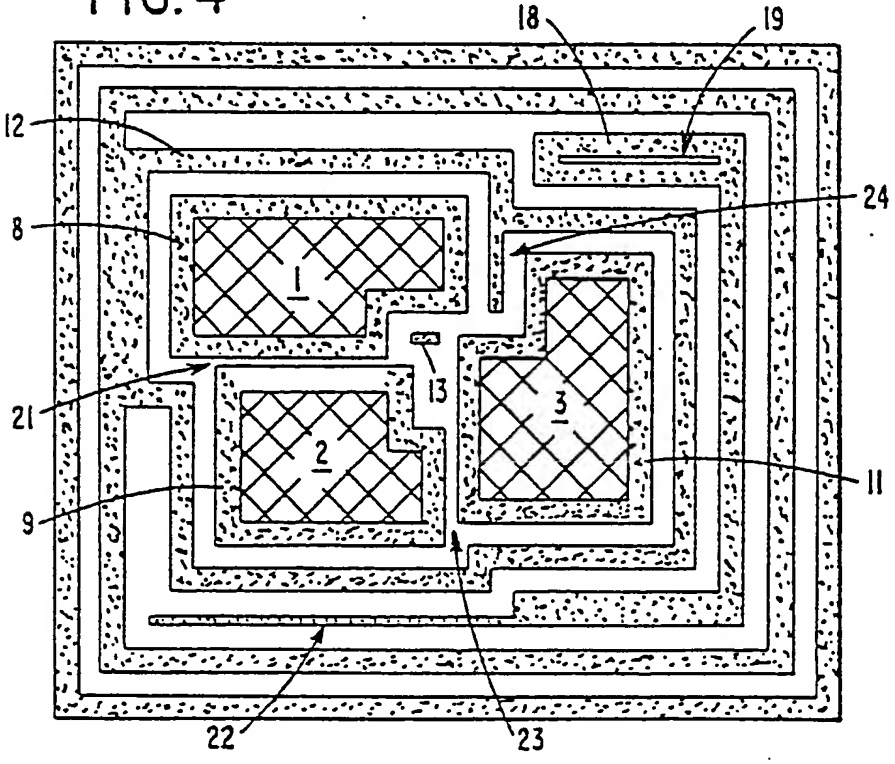


FIG. 5

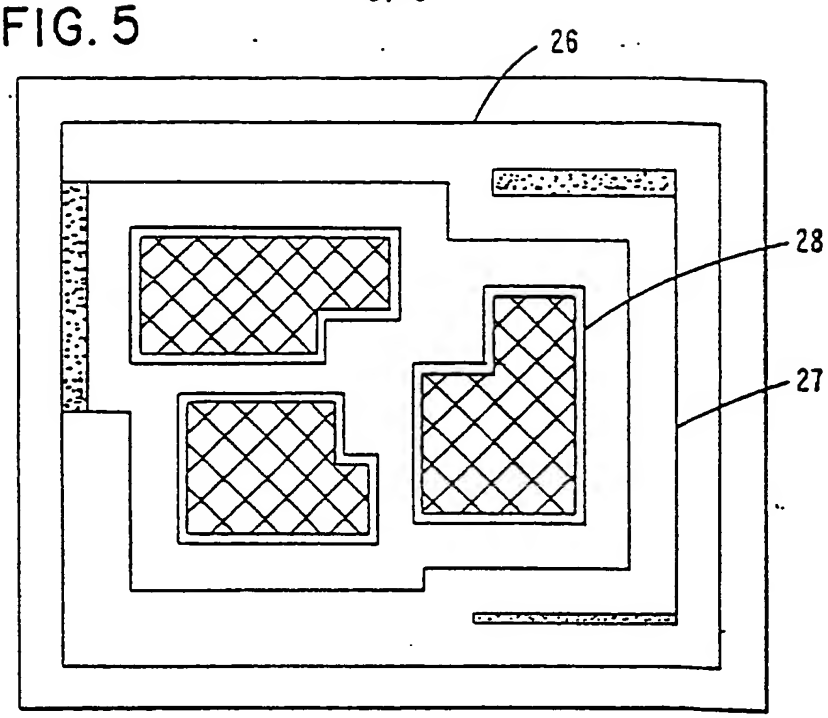


FIG. 6

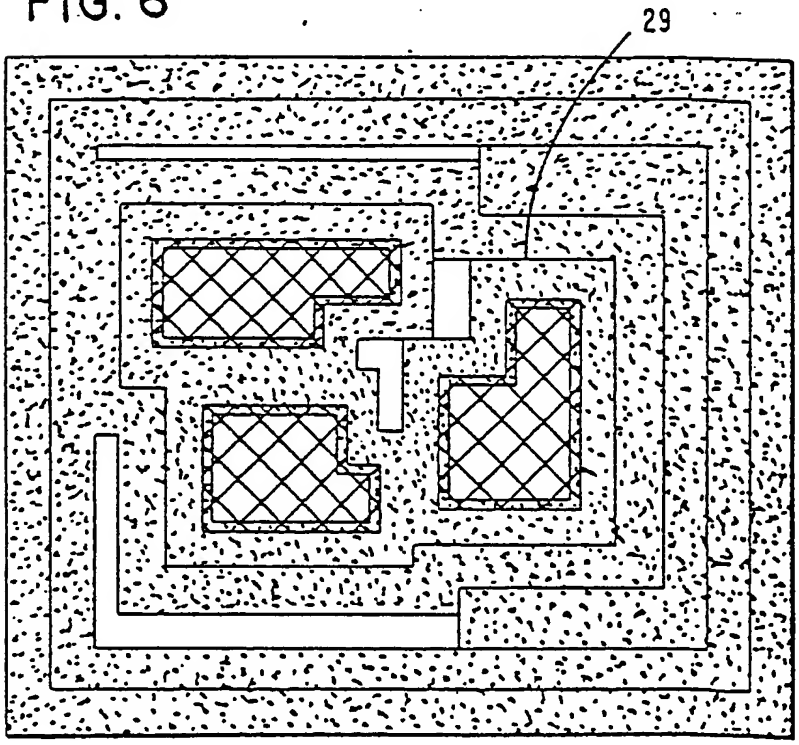


FIG. 7

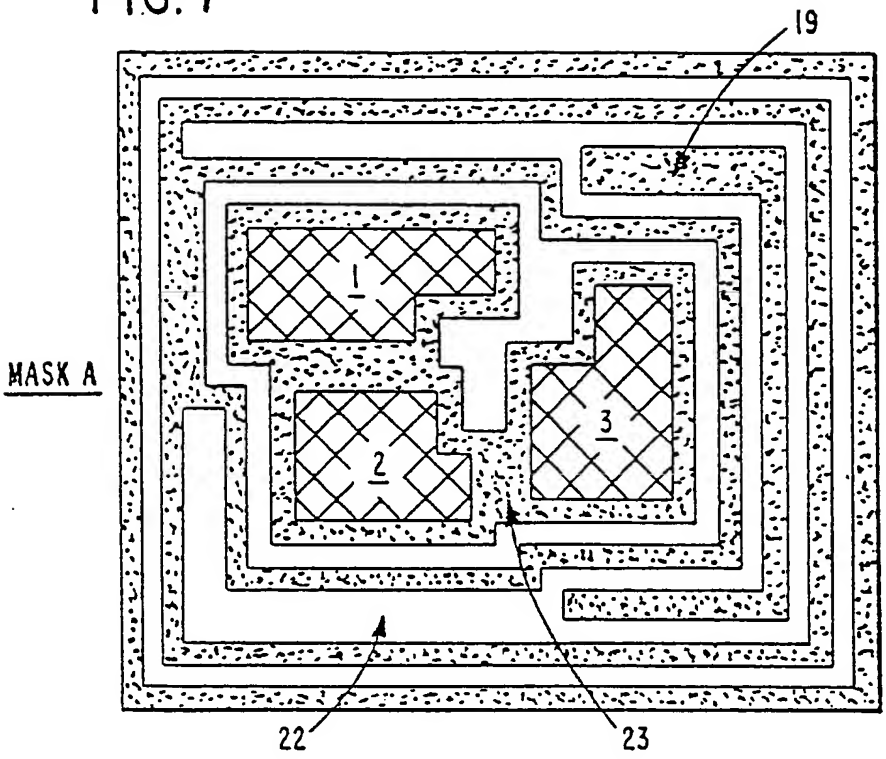


FIG. 8

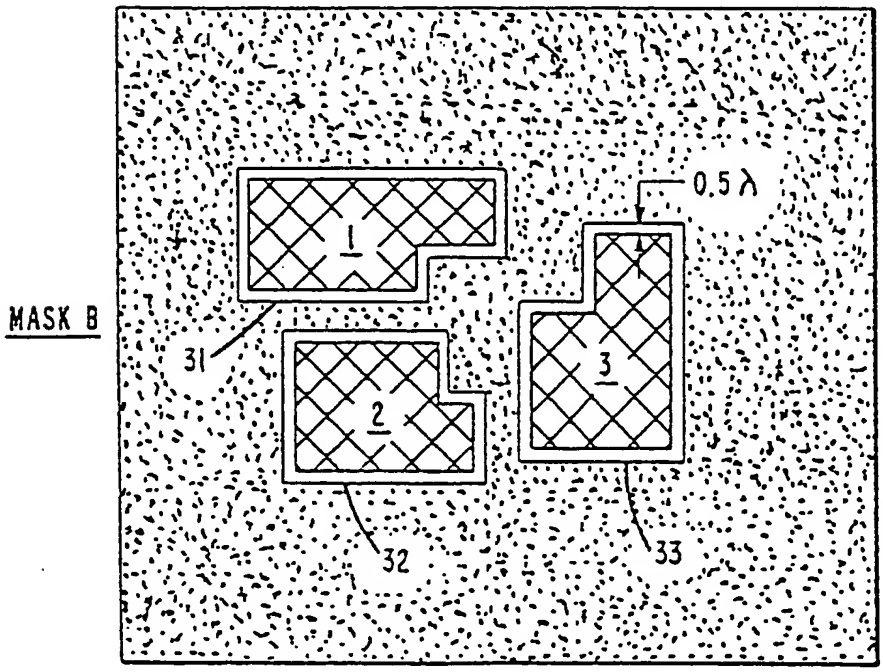


FIG. 9

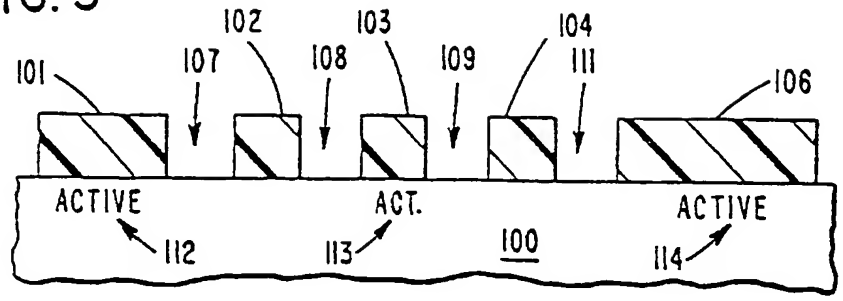


FIG. 10

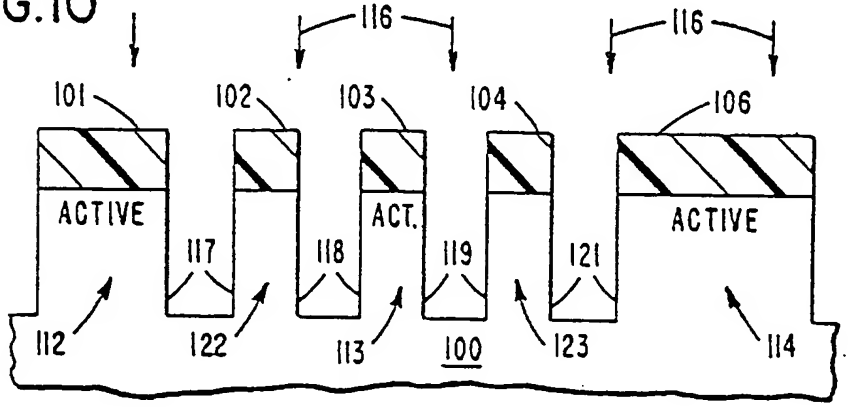


FIG. 11

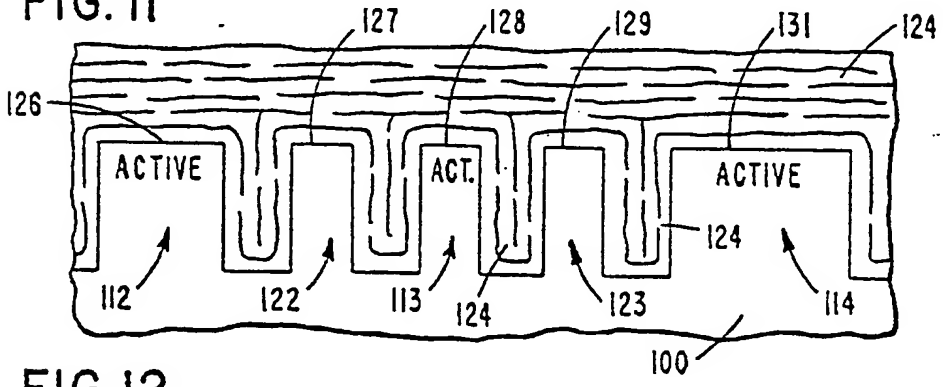


FIG. 12

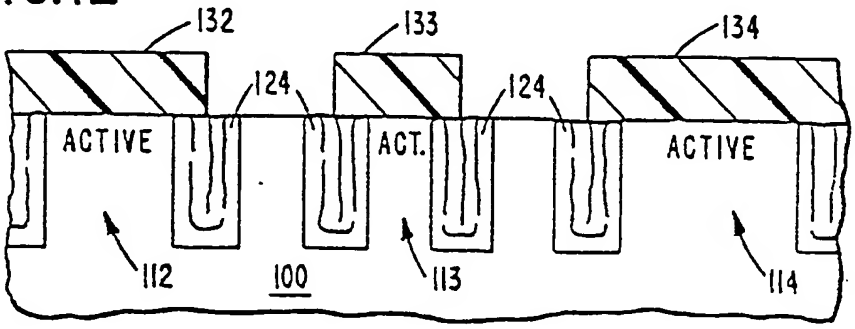


FIG. 13

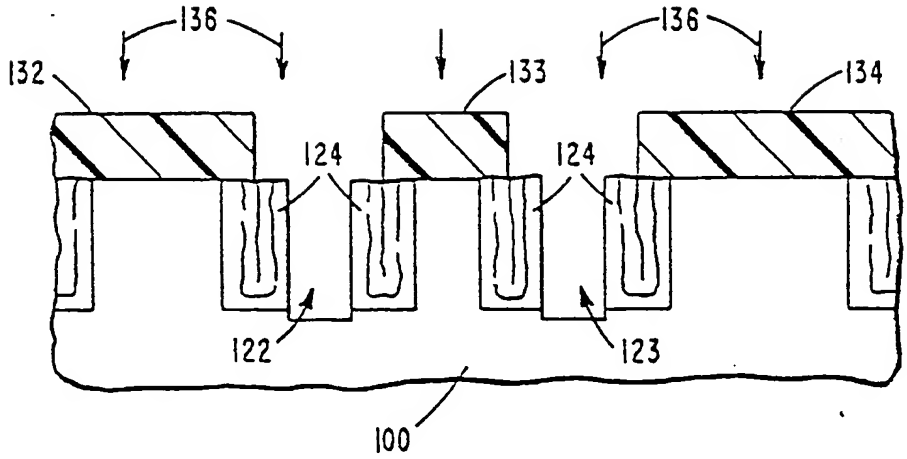


FIG. 14

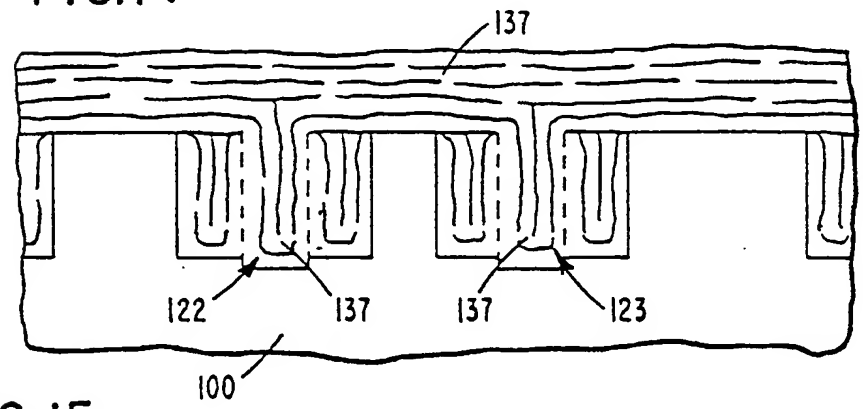
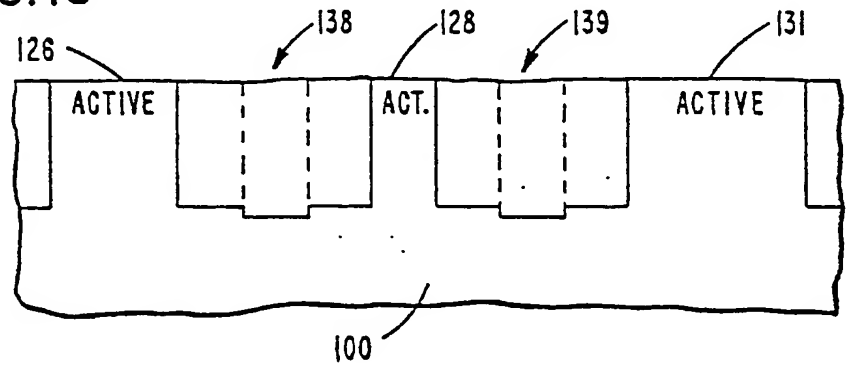


FIG. 15



PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 : H01L 21/76 | A3

(11) International Publication Number: WO 87/ 03139

(43) International Publication Date: 21 May 1987 (21.05.87)

(21) International Application Number: PCT/US86/02395

(22) International Filing Date: 10 November 1986 (10.11.86)

(31) Priority Application Number: 798,511

(32) Priority Date: 15 November 1985 (15.11.85)

(33) Priority Country: US

(71) Applicant: NCR CORPORATION [US/US]; World Headquarters, Dayton, OH 45479 (US).

(72) Inventors: ELLSWORTH, Daniel, Lloyd ; 1424 Linden Lake Road, Fort Collins, CO 80524 (US). CRAVENS, Scott, Harris ; 4455 Hollyhock Street, Fort Collins, CO 80526 (US). MOLL, Maurice, Michael ; 742 Larkbunting Drive, Fort Collins, CO 80526 (US).

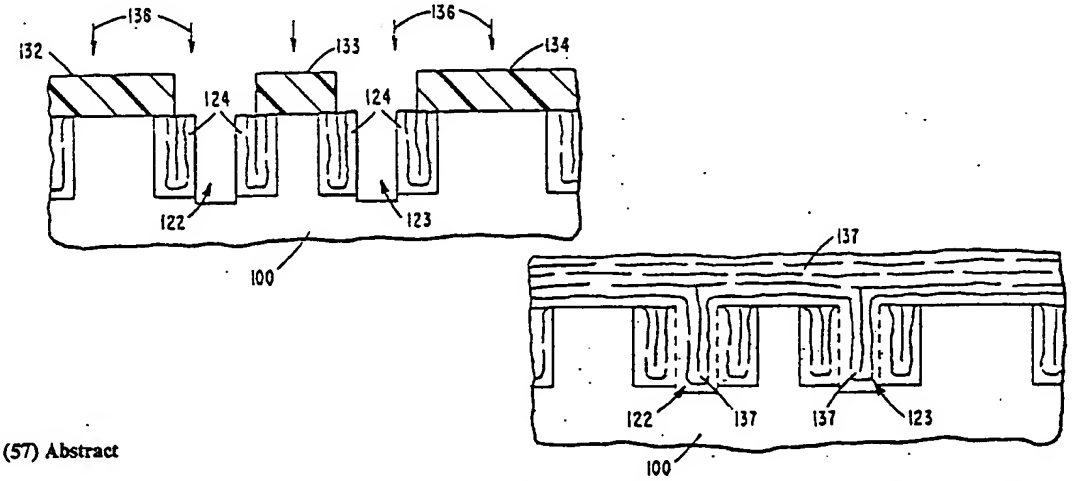
(74) Agents: SALYS, Casimer, K. et al.; Law Department, Intellectual Property Section, NCR Corporation, World Headquarters, Dayton, OH 45479 (US).

(81) Designated States: DE (European patent), FR (European patent), GB (European patent), JP, NL (European patent).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report: 27 August 1987 (27.08.87)

(54) Title: PROCESS FOR TRENCH OXIDE ISOLATION OF INTEGRATED DEVICES



(57) Abstract

In a process for forming dielectrically filled planarized trenches (4; 138, 139) of arbitrary width in a semiconductor substrate (100), a first mask (A) defines active regions (112-114) and subdivides the trench isolation regions into a succession of the trench and plateau regions, where the widths of the trench and plateau regions fall within a dimensional range constrained by the photolithographic precision of the masks and the ability to conformally deposit dielectric material into the trenches. With the first etch mask (A) in place, the substrate (100) is anisotropically etched to form first trenches (117, 118, 119, 121). A conformal deposition of dielectric (124) follows, to form substantially void free trench dielectric, following which the surface is planarized. Next, a second mask (B), defined to be slightly larger than the active regions (112-114), is formed over the substrate (100). A selective etch is then applied to remove the plateau regions (122, 123) and thereby form new trenches approximating in depth the first trenches. A second conformal deposition of dielectric (137) follows, whereafter the surface is again planarized. The substrate surface is now planar and divided into active regions (1-3; 112-114) which are separated by oxide filled, arbitrary width trenches (4; 138, 139).

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria
AU	Australia
BB	Barbados
BE	Belgium
BG	Bulgaria
BJ	Benin
BR	Brazil
CF	Central African Republic
CG	Congo
CH	Switzerland
CM	Cameroon
DE	Germany, Federal Republic of
DK	Denmark
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
HU	Hungary
IT	Italy
JP	Japan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
LI	Liechtenstein
LK	Sri Lanka
LU	Luxembourg
MC	Monaco
MG	Madagascar
ML	Mali
MR	Mauritania
MW	Malawi
NL	Netherlands
NO	Norway
RO	Romania
SD	Sudan
SE	Sweden
SN	Senegal
SU	Soviet Union
TD	Chad
TG	Togo
US	United States of America

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 86/02395

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 21/76

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	EP, A, 0091984 (K.K. TOSHIBA) 26 October 1983 see page 6, line 1 - page 17, line 5; figures 22A-22J	1,4,5,7,9, 11-13
A		2,3,6,14,15
Y		8
	--	
A	IBM Technical Disclosure Bulletin, volume 25, no. 11B, April 1983, (New York, US), P.J. Tsang: "Forming wide trench dielectric isolation", pages 6129-6130 see figures 1-8	1,5,7
Y		8
	--	
A	US, A, 4472240 (S. KAMEYAMA) 18 September 1984 see column 12, line 56 - column 13, line 23; claims 1-10,13	1-15
	--------	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
21st July 1987	28. 07. 87
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 86/02395 (SA 15473)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 23/07/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A- 0091984	26/10/83	JP-A-	58048437	22/03/83
		US-A-	4491486	01/01/85
		JP-A-	58061642	12/04/83
US-A- 4472240	18/09/84	JP-A-	58032430	25/02/83
		JP-A-	58034917	01/03/83
		JP-A-	58131747	05/08/83

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☑ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☑ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.